What is claimed is:

1. A memory cell for a memory array in a folded bit line configuration, the memory cell comprising:

an access transistor formed in a pillar of single crystal semiconductor material, the access transistor having first and second source/drain regions and a body region that are vertically aligned;

the access transistor further including a gate coupled to a word line disposed adjacent to the body region;

a passing word line separated from the gate by an insulator for coupling to other memory cells adjacent to the memory cell; and

a trench capacitor, wherein the trench capacitor includes a first plate that is formed integral with the first source/drain region of the access transistor and a second plate that is disposed adjacent to the first plate and separated from the first plate by a gate oxide.

2. The memory cell of claim 1, wherein the second plate of the trench capacitor surrounds the second source/drain region.

3. The memory cell of claim 1, wherein the second plate comprises poly-silicon.

4. The memory cell of claim 1, and further comprising an ohmic contact that couples the second plate to a layer of semiconductor material.

5. A memory device, comprising:

an array of memory cells, each memory cell including a vertical access transistor formed of a single crystalline semiconductor pillar that extends outwardly from a substrate with body and first and second source/drain regions, a gate disposed adjacent

to a side of the pillar adjacent to the body region and a trench capacitor wherein a first plate of the trench capacitor is integral with the first source/drain region and a second plate of the trench capacitor is disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at the second source/drain region of the access transistor so as to form columns of memory cells in a folded bit line configuration; and

a number of word lines disposed substantially orthogonal to the bit lines in trenches between rows of the memory cells, wherein each trench includes two word lines, each word line coupled to gates of alternate access transistors on opposite sides of the trench.

6. The memory device of claim 5, wherein the pillars extend outwardly from a semiconductor portion of the substrate.

7. The memory device of claim 5, wherein a surface area of the memory cell is $4F^2$, where F is a minimum feature size.

8. The memory device of claim 5, wherein the second plate of the trench capacitor surrounds the second source/drain region of the access transistor.

9. The memory device of claim 5, wherein the second plate of the trench capacitor is maintained at approximately ground potential.

10. The memory device of claim 5, wherein the second plate of the trench capacitor comprises poly-silicon that is maintained at a constant potential.

11. The memory device of claim 5, wherein the pillar has a sub-micron width so as to allow substantially full depletion of the body region.

12. The memory device of claim 5, wherein the word lines are sub-lithographic.

13. A memory array comprising:

a number of memory cells forming an array with a number of rows and columns, each memory cell including an access transistor having body and first and second source/drain regions formed vertically, outwardly from a substrate and a gate disposed adjacent to a side of the transistor, the second source/drain region including an upper semiconductor surface;

a number of first isolation trenches separating adjacent rows of memory cells;

first and second word lines disposed in each of the first isolation trenches and coupled to alternate gates on opposite sides of the trench; and

a number of second isolation trenches, each substantially orthogonal to the first isolation trenches and interposed between adjacent memory cells.

14. The memory array of claim 13, wherein the gates of the access transistors are each formed integral with one of the word lines.

15. The memory array of claim 13, wherein the pillars extend outwardly from a semiconductor portion of the substrate.

16. The memory array of claim 13, wherein a surface area of the memory cell is $4F^2$, where F is a minimum feature size.

17. The memory array of claim 13, wherein the second plate of the trench capacitor surrounds the second source/drain region of the access transistor.

18. The memory array of claim 13, wherein the second plate of the trench capacitor comprises poly-silicon that is maintained at a constant potential.

19. The memory array of claim 13, wherein the word lines have a width that is less than the minimum feature size, F.

20. A method of fabricating a memory array, the method comprising the steps of :

forming a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein the access transistor includes a first source/drain region, a body region and a second source/drain region formed vertically thereupon;

forming a trench capacitor, wherein a first plate of the trench capacitor is integral with the first source/drain region of the access transistor;

forming a number of word lines in a number of trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench; and

forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

21. The method of claim 20, wherein the step of forming a trench capacitor further includes the step of forming a second plate that surrounds the first plate.

22. The method of claim 20, and further comprising the step of forming a contact that couples a second plate of the trench capacitor to an underlying semiconductor layer.

23. The method of claim 20, where the step of forming a trench capacitor comprises the step of forming a second plate that forms a grid pattern in a layer of semiconductor material such that the grid surrounds each of the pillars that form the access transistors.

24. The method of claim 20, wherein the step of forming a trench capacitor comprises the step of depositing poly-silicon in crossing row and column isolation trenches formed around the pillars that define the access transistors.

25. A method of fabricating a memory array, the method comprising the steps of:

forming a first conductivity type first source/drain region layer on a substrate;

forming a second conductivity type body region layer on the first source/drain region layer;

forming a first conductivity type second source/drain region layer on the body region layer;

forming a plurality of substantially parallel column isolation trenches extending through the second source/drain region layer, the body region layer, and the first source/drain region layer, thereby forming column bars between the column isolation trenches;

forming a plurality of substantially parallel row isolation trenches, orthogonal to the column isolation trenches, extending to substantially the same depth as the column isolation trenches, thereby forming an array of vertical access transistors for the memory array;

filling the row and column isolation trenches with a conductive material to a level that does not exceed the lower level of the body region so as to provide a common plate for capacitors of memory cells of the memory array;

forming two conductive word lines in each row isolation trenches that selectively interconnect alternate access transistors on opposite sides of the row isolation trench; and

forming bit lines that selectively interconnect the second source/drain regions of the access transistors on each column.

26. The method of claim 25, wherein the step of forming a first conductivity type first source/drain region layer on a substrate comprises the step of forming first

conductivity type first source/drain region layer on a substrate that extends outwardly from the substrate to a distance sufficient for the source/drain region layer to also function as a first plate of the capacitor for each memory cell in the array.